IN THE CLAIMS

1.   (Previously Presented) A multi-processor system, comprising:

a plurality of processors, each processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit having an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory;

an external switch coupled to each of the plurality of processors, the external switch operable to pass data to and from any of the plurality of processors, the external switch including an external directory, the external directory operable to provide a memory reference for each of the plurality of processors to remote data that is not provided within its own integrated memory directory.

2.   (Original) The multi-processor of Claim 1, wherein the integrated memory directory is a cache buffer operable to hold a plurality of most recently accessed memory references.

3.   (Original) The multi-processor system of Claim 2, wherein the integrated memory directory is operable to overwrite an oldest memory reference with a new memory reference upon reaching a buffer limit.

4.   (Original) The multi-processor of Claim 1, wherein the integrated memory directory of a particular processor is operable to hold memory references to data stored at other processors.

5.   (Original) The multi-processor system of Claim 1, wherein the external directory is operable to receive a request for directory assistance from a particular one of the plurality of processors, the directory assistance request including a request for data not having a memory reference in the integrated memory directory of the particular one of the plurality of processors.

6.   (Original) The multi-processor system of Claim 5, wherein the external directory is operable to generate a memory reference for the requested data.

7.   (Original) The multi-processor device of Claim 5, wherein the external switch is operable to provide the generated memory reference to the integrated memory directory of the particular one of the plurality of processors in accordance with the request for data.

8.   (Original) The multi-processor system of Claim 5, wherein the external switch is operable to provide the requested data to the particular one of the processors in response to the generated memory reference.

9.   (Original) The multi-processor of Claim 1, wherein each of the plurality of processors includes an integrated network interface operable to communicate information to and from the external switch.

10.   (Original) The multi-processor system of Claim 1, wherein the memory references in the external directory are represented in a same manner as memory references in a particular integrated memory directory.

11.   (Previously Presented) A method of accessing data in a multi-processor system, comprising:

storing information in a local memory, the local memory being integrated within a particular one of a plurality of processors of the multi-processor system;

maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors;

generating a request for data;

determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory;

forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory;

identifying a memory reference for the data in response to the request;

obtaining the data from the remote memory via the external switch in response to the identified memory reference.

12.   (Original) The   method of   Claim   11,   further
comprising:

    obtaining the memory reference to the data stored in the
remote memory.

13.   (Original) The method of Claim 11, wherein the local
memory is integrated with a particular one of a plurality of
processors of the multi-processor system, the list of memory
references being maintained in a memory directory integrated
with the local memory in the particular one of the plurality
of processors.

14.   (Original) The method of Claim 13, wherein the
identified memory reference is generated external to the
particular one of the plurality of processors.

15.   (Original) The method of Claim 13, wherein the
memory reference is to data stored at a processor different
from the particular one of the plurality of processors.

16.   (Previously Presented) A processor in a multi-processor system, comprising:

a local memory integrated in the processor and operable to provide/receive/store data;

a central processing unit;

a memory controller integrated in the central processing unit and operable to control access to and from the local memory;

a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to generate a data request for data not having a memory reference in the memory directory;

a network interface integrated in the processor and operable to provide the data request to an external directory external to the processor, the network interface operable to receive the data according to the data request.

17.   (Original) The processor of Claim 16, wherein the memory directory maintains a list of most recently accessed memory references.

18.   (Original) The processor of Claim 16, wherein the local memory has a capacity of four gigabytes of data and the memory directory has a capacity of eight megabytes of data memory reference.

19.   (Original) The processor of Claim 16, wherein the network interface is operable to provide a memory reference generated by the external directory to the memory directory.

20.   (Original) The processor of Claim 16, wherein the memory directory includes two to the power of eighteen memory references.